What is claimed is:

[Claim 1] 1. A method for programming a non-volatile memory, comprising:

selecting a reference level according to a level distribution of a plurality of memory cells in a storage state in the non-volatile memory; and

programming a plurality of predetermined memory cells to a next storage state according to the reference level, wherein

the reference level falls between the cell level distribution of the memory cells in the current storage state and the cell level distribution of the memory cells in the next storage state.

[Claim 2] 2. The method of claim 1, wherein the levels of the memory cells in the next storage state are higher than the levels of the memory cells in the current storage state, and the reference level falls between a highest level of the memory cells in the current storage state and a lowest level of the memory cells in the next storage state.

[Claim 3] 3. The method of claim 2, wherein selecting the reference level comprises:

predetermining a plurality of candidate reference levels; and

selecting one candidate reference level from the candidate reference levels whose levels are higher than the highest level of the memory cells in the storage state as the reference level.

[Claim 4] 4. The method of claim 1, wherein the non-volatile memory is a one-time programmable (OTP) memory, a multi-time programmable (MTP) memory, a multi-level cell (MLC) memory, or a programmable resistor with erase-less memory (PREM).

[Claim 5] 5. The method of claim 1, wherein the storage state of a memory cell depends on its cell current, and the reference level is a current reference level.

[Claim 6] 6. The method of claim 1, wherein the storage state of a memory cell depends on its threshold voltage, and the reference level is a threshold voltage reference level.

[Claim 7] 7. A method for programming a multi-level cell (MLC) non-volatile memory whose memory cells having a first storage state up to an N^{th} storage state in an ascending order of level, the method comprising:

(a) selecting an i^{th} reference level according to a level distribution of the memory cells in an i^{th} storage state;
(b) programming a plurality of memory cells to a $(i+1)^{th}$ storage state according to the i^{th} reference level; and
repeating steps (a) and (b) until programming of the N^{th} storage state is completed, wherein an initial value of i is 1, the value of i is incremented by 1 before each repetition, and the i^{th} reference level falls between a highest level of the memory cells in the i^{th} storage state and a lowest level of the memory cells in the $(i+1)^{th}$ storage state.

[Claim 8] 8. The method of claim 7, further comprising:

predetermining a plurality of candidate reference levels before steps (a) and (b);
and step (a) comprising:
selecting one candidate reference level from the candidate reference levels whose levels are higher than a highest level of the memory cells in the i^{th} storage state as an i^{th} reference level.

[Claim 9] 9. The method of claim 7, wherein the storage state of a memory cell depends on its threshold voltage, and the reference level is a threshold voltage reference level.

[Claim 10] 10. The method of claim 7, wherein the storage state of a memory cell depends on its cell current, and the reference level is a current reference level.

[Claim 11] 11. The method of claim 10, wherein the MLC non-volatile memory comprises a programmable resistor with erase-less memory (PREM).

[Claim 12] 12. A method for programming a multi-time programmable (MTP) non-volatile memory, comprising:

selecting a reference level according to a level distribution of memory cells of the MTP non-volatile memory;
resetting a storage state of each of the memory cells to a first storage state; and
programming a plurality of predetermined memory cells to a second storage state according to the reference level,
wherein the reference level falls between a highest level of the memory cells in the first storage state and a lowest level of the memory cells in the second storage state.

[Claim 13] 13. The method of claim 12, wherein selecting the reference level comprises:

predetermining a plurality of candidate reference levels; and
selecting one candidate reference level from the candidate reference levels whose level are higher than the highest level of the memory cells as the reference level.

[Claim 14] 14. The method of claim 12, wherein the storage state of a memory cell depends on its threshold voltage, and the reference level is a threshold voltage reference level.

[Claim 15] 15. The method of claim 12, wherein the storage state of a memory cell depends on its cell current, and the reference level is a current reference level.

[Claim 16] 16. The method of claim 15, wherein the MTP non-volatile memory comprises a programmable resistor with erase-less memory (PREM).